REMARKS

In the interest of clarity, the Item Numbers below correspond to the Examiner's Item Numbers in the Office Action.

1. With this Response, Applicant has added claims 76-81. Thus, Claims 1-30, 34, and 76-81 are pending, which Applicant will presently discuss.

2. The Examiner objected to various informalities in Claims 1, 5, 9, and 14-17.

In Claim 1 (line 7), the Examiner suggested changing "a synchronous mirror delay" to "the synchronous mirror delay circuit. Applicant disagrees with the necessity of using only definite articles (i.e., "the") in claim elements that are earlier mentioned in a non-limiting preamble. Nevertheless, Applicant has changed the preamble of Claim 1 to eliminate the phrase "a synchronous mirror delay circuit," thus rendering this objection as moot.

In Claim 5 (line 6), the Examiner suggested changing "a synchronous mirror delay circuit" to "the synchronous mirror delay circuit." Applicant disagrees with the necessity of using only definite articles (i.e., "the") in claim elements that are earlier mentioned in a non-limiting preamble. Nevertheless, Applicant has changed the preamble of Claim 5 to eliminate the phrase "a synchronous mirror delay circuit," thus rendering this objection as moot. In addition, Applicant also deleted the word "circuit" following the phrase "synchronous mirror delay (SMD)" (on line 7) as redundant since the SMD is, in fact, a circuit. Also, in line 7, the Examiner suggested deleting the word "in." While Applicant disagrees with the necessity of doing so, Applicant respectfully made the change (at line 8).

In Claim 9 (lines 7-8), the Examiner suggested changing "a synchronous mirror delay" to "the synchronous mirror delay." Applicant disagrees with the necessity of using only definite articles (i.e., "the") in claim elements that are earlier mentioned in a non-limiting preamble. Nevertheless, Applicant has changed the preamble of Claim 9 to eliminate the phrase "a synchronous mirror delay circuit," thus rendering this objection as moot.

In Claim 14 (line 1), Applicant harmonized the preamble with the preamble in Claim 13, as requested.

In Claims 15-17, Applicant harmonized the preambles with the preamble in Claim 13, as requested.

Applicant has made other various corrections where suggested.

3. The Examiner rejected **Claims 13-18 and 23-25** under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. More specifically, the Examiner asserts that the decoder 30 and multiplexors 28 and 46 are "critical or essential to the practice of the invention, but not included in the claims or a circuit without these elements is not enabled by the disclosure." Respectfully, Applicant traverses and requests withdrawal.

As per Claim 13, the Examiner has also asserted that "the specification does not enable a phase detector connected to a SMD circuit as recited, i.e., as shown in Fig. 1 of the present invention, the phase detector 26 is not connected to the SMD 12." Applicant has amended Claim 13 to specify that the phase detector is in "electronic communication" with the SMD, as representatively illustrated in Fig. 1 and described throughout the Specification.

Regarding whether the elements decoder 30 and multiplexors 28, 46 must be included in the claim as being "critical," Applicant respectfully directs the Examiner's attention to FIG. 7 and the following description thereof:

> Although a specific logic arrangement is shown, it is contemplated that any suitable control logic may be used to define the conditions of the signals and then selecting them accordingly...Selector 238 selects, based on the input 240 from the phase detector 226, whether to put signal 242 or 244 to input 246 into clock tree driver 248.

See Fig. 7 and Page 11, lines 14-23. As disclosed, it is not required that the memory device of Claim 13 be limited to control logic embodied as decoders and multiplexors, but applies to more generic functionality embodied as the representative selector 238. Applicant has added new claim 76 to illustrate that in one preferred embodiment, the phase detector is in electronic communication with the SMD through at least one of a decoder and one or more multiplexors. Applicant has also added new claim 77 to illustrate that in another preferred embodiment, the phase detector is in electronic communication with the SMD through a decoder and one or more multiplexors.

As per Claims 14-17, the Examiner rejected these claims for the same reasons as noted in Claim 13. Respectfully, Applicant traverses and requests withdrawal. More specifically, Applicant notes that since Claims 14-17 depend from Claim 13, and Applicant's belief that Applicant's arguments have successfully overcome the Examiner's rejection of Claim 13, any further rejection to Claims 14-17 is thereby obviated and rendered moot.

As per Claim 18, the Examiner rejected the claim for the same reasons noted in Claim 13. More specifically, the Examiner presumably asserts that decoders and multiplexors are critical elements and must therefore be included in the claim. Respectfully, Applicant traverses and requests withdrawal. More specifically, Applicant asserts that it is not required that the SMD system of Claim 18 be limited to control logic embodied as decoders and multiplexors, but applies to more generic functionality embodied as the representative selector 238 in Fig. 7, as previously elaborated upon with respect to Claim 13. Applicant has added new claim 78 to illustrate that in one preferred embodiment, the phase detector is associated with the SMD through at least one of a decoder and one or more multiplexors. Applicant has also added new claim 79 to illustrate that in another preferred embodiment, the phase detector is associated with the SMD through a decoder and one or more multiplexors. In much the same way Applicant asserts that the phase detector is in "electronic communication" with the SMD in Claim 13, Applicant further asserts that the phase detector is also "associated with" the SMD as recited in Claim 18 (line 3), as representatively illustrated in Fig. 1 and described throughout the Specification. Accordingly, further amendment of Claim 18 is not deemed necessary.

As per Claims 23-25, the Examiner rejected these claims for the same reasons noted in Claim 13. More specifically, the Examiner presumably asserts that decoders and multiplexors are critical elements and must therefore be included in the claim. Respectfully, Applicant traverses and requests withdrawal. More specifically, Applicant asserts that the SMD system of Claim 23 is **not** limited to control logic embodied as decoders and multiplexors, but applies to more generic functionality embodied as the representative selector 238 in Fig. 7, as previously elaborated upon with respect to Claim 13. Applicant has added new claim 80 to illustrate that in one preferred embodiment, the phase detector is in operational association with the SMD through at least one of a decoder and one or more multiplexors. Applicant has also added new claim 81 to illustrate that in another preferred embodiment, the phase detector is in operational association with the SMD through a decoder and one or more multiplexors. In much the same way Applicant asserts that the phase detector is in "electronic communication" with the SMD in Claim 13, Applicant further asserts that the phase detector is in "operational association" with the SMD in Claim 23 (line 3), as representatively illustrated in Fig. 1 and described throughout the Specification. Accordingly, further amendment of Claim 23 is not deemed necessary.

Insofar as Claims 24-25 depend from Claim 23, and Applicant's belief that Applicant's arguments have successfully overcome the Examiner's rejection of Claim 23, any further rejection to Claims 24-25 is thereby obviated and rendered moot.

4. The Examiner rejected **Claims 13-30 and 34** under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Respectfully, Applicant traverses and requests withdrawal.

As per Claim 13, the Examiner asserts that "the phase detector is *not* connected to the SMD as recited, but rather, it is used for determining whether CIN or CIN' is used as an input to the SMD or bypassed the SMD altogether..." Applicant has amended Claim 13 to specify that the phase detector is in "electronic communication" with the SMD, as previously elaborated upon.

The Examiner further rejected Claim 13 as being incomplete for omitting essential elements and structural relationships between these elements, such omissions allegedly amounting to a gap between the elements, the omitted elements allegedly being the decoder, multiplexors, and their structural relationships to the rest of the circuits. Respectfully, Applicant traverses and requests withdrawal for the reasons previously presented above in addressing the rejection of Claim 13 under § 112 (1).

The Examiner further asserted that the recitation "at least one of the conditions reduces a number of effective delay stages in the SMD" on the last line appears misdescriptive because the delay stages in the SMD are physical stages. Applicant has amended Claim 13 to specify that for at least one of the conditions, a number of delay stages is reduced for a selected signal to pass through the memory device.

As per Claims 14-17, the Examiner rejected these claims for the same reasons as noted in Claim 13. Respectfully, Applicant traverses and requests withdrawal. More specifically, Applicant notes that since Claims 14-17 depend from Claim 13, and Applicant's belief that Applicant's arguments have successfully overcome the Examiner's rejection of Claim 13, any further rejection to Claims 14-17 is thereby obviated and rendered moot.

As per Claim 18, the Examiner rejected the claim for the same reasons noted in Claim 13. Respectfully, Applicant traverses and requests withdrawal. In much the same way Applicant asserts that the phase detector is in "electronic communication" with the SMD in

Claim 13, Applicant further asserts that the phase detector is also "associated with" the SMD in Claim 18 (line 3), as previously elaborated upon in addressing the rejection of Claims 13 and 18 under § 112 (1).

As per Claim 19, the Examiner asserts that the recitation on line 4 is misdescriptive because "it does not make any sense to recite a node related to a signal." Applicant has amended Claim 19 to specify that the input buffer receives the external clock signal to produce CIN, CIN', and CDLY. Explicit support for this amendment is found in the Specification, to wit, "An external clock signal 16 is input into receiver and buffer 18. This produces clock input signal 20 (CIN), inverted clock input signal (CIN') 21 and clock delay signal 22 (CDLY)." *Page 5, lines 15-18.* Thus, instead of a node relating to a signal, Claim 19 now recites that the input buffer receives the external clock signal to produce CIN, CIN', and CDLY.

In addition, the Examiner further asserted that the recitation "at least one of the conditions reduces a number of effective delay stages in the SMD" on the last line of Claim 19 appears misdescriptive because the delay stages in the SMD are physical stages. Applicant has amended Claim 19 to specify that for at least one of the phases, a number of delay stages is reduced for a selected signal to pass through the circuit.

As per Claims 20-22, the Examiner rejected these claims for the same reasons as noted in Claim 19. Respectfully, Applicant traverses and requests withdrawal. More specifically, however, Applicant notes that since Claims 20-22 depend from Claim 19, and Applicant's belief that Applicant's arguments have successfully overcome the Examiner's rejection of Claim 19, any further rejection to Claims 20-22 is thereby obviated and rendered moot.

As per Claims 23-25, the Examiner rejected these claims for the same reasons as noted in Claims 13, 16, and 14, respectively. Respectfully, Applicant traverses and requests withdrawal.

More specifically, in regards to rejecting Claim 23 for the same reasons noted in Claim 13, the Examiner rejected Claim 13 for three reasons: i) the Examiner asserted that the phase detector is not connected to the SMD, ii) the Examiner asserted the claim was incomplete for omitting essential elements and structural relationships between these elements, such omissions allegedly amounting to a gap between the elements, the omitted elements allegedly being the decoder, multiplexors, and their structural relationships to the rest of the circuits; and iii) the Examiner asserted that the recitation "at least one of the conditions reduces a number of

effective delay stages in the SMD" on the last line appears misdescriptive because the delay stages in the SMD are physical stages. As to the first point (i.e., unconnected elements), in much the same way Applicant asserts that the phase detector is in "electronic communication" with the SMD in Claim 13, Applicant further asserts that the phase detector is in "operational association" with the SMD in Claim 23 (line 3), as previously elaborated upon in addressing the rejection of Claim 23 under § 112 (1). As to the second point (i.e., omitted elements), Applicant asserts, as previously elaborated upon, elements have not been omitted. Nevertheless, Applicant added new claims 80-81, as previously elaborated upon. As to the third point (i.e., misdescriptive last line), Applicant has amended Claim 23 to specify that a number of delay stages is reduced for a selected signal to pass through the SMD.

In regards to the rejection of Claim 24 for the same reason noted in Claim 16, Applicant notes that since Claim 24 depends from Claim 23, and Applicant believes that Applicant's arguments have successfully overcome the Examiner's rejection of Claim 23, any further rejection to Claim 24 is thereby obviated and rendered moot.

In regards to the rejection of Claim 25 for the same reason noted in Claim 14, Applicant notes that Claim 14 was rejected for the same reasons noted in Claim 13. As for the three reasons given for rejecting Claim 13, only the third reason appears applicable to the language of Claim 25, that is, that the recitation "the number of effective delay stages of the SMD is reduced" on the last line is misdescriptive. Applicant requests clarification from the Examiner if this assumption is mistaken. In response, however, Applicant has amended Claim 25 to specify that for the second phase, the number of delay stages is reduced for a selected signal to pass through the SMD.

As per Claim 26, the Examiner asserted that the recitation on the last four lines is unclear and not understood. Applicant has amended Claim 26 to delete the word "and" (at line 6) before the wherein clause to specify that the limitations following the wherein clause are not structural elements. Rather, the "phase detection and selection circuit" recited in the last four lines describe selectively feeding CIN or CIN' into a SMD based upon output signal combinations wherein a number of delay stages is reduced for a selected signal to pass through the system, which find elements and/or structure for support earlier in the language of the claim.

The Examiner also asserted that the recitation "wherein a number of effective delay stages is reduced" on the last line appears misdescriptive because the delay stages in the SMD

are physical stages. Applicant has amended Claim 26 to specify that a number of delay stages is reduced for a selected signal to pass through the system.

As per Claims 27-30, the Examiner rejected these claims for the same reasons as noted in Claim 19. Respectfully, Applicant traverses and requests withdrawal. More specifically, Applicant notes that since Claim 27 depends from Claim 26 and Claims 28-30 depend from Claim 27, and Applicant believes that Applicant's arguments have successfully overcome the Examiner's rejection of Claim 26, any further rejection to Claims 27-30 is thereby obviated and rendered moot.

As per Claim 34, the Examiner asserted that "the functional recitation on the last four lines does not have any elements and/or structure to support." Applicant has amended Claim 34 to delete the word "and" (at line 14) before the wherein clause to specify that the limitations following the wherein clause are not structural elements. Rather, the "timing conditions" recited in the last four lines describe the timing conditions of lines 10 and 14. Similarly, CIN, CDLY, and the SMD also find elements and/or structure for support earlier in the language of the claim.

5. Applicant thanks the Examiner for considering Applicant's earlier arguments with respect to the claims.

6. The Examiner indicates Claims 1-12 are allowed after the objections noted in § 2 are overcome. Fully believing Applicant has overcome the objections noted in section 2, Applicant respectfully submits that these claims should now be allowed.

7. The Examiner indicates Claims 19-22, 26-30, and 34 would be allowable if rewritten to overcome the rejections(s) under 35 U.S.C. 112, second paragraph. Fully believing Applicant has overcome the rejections(s) under 35 U.S.C. 112, second paragraph, Applicant respectfully submits that these claims should now be allowed.

8. Applicant believes Applicant has taken steps to overcome any perceived indefiniteness problems noted in the Office Action regarding Claims 13-18 and 23-25. Fully believing Applicant has overcome any perceived indefiniteness problems, Applicant respectfully submits that these claims should now be allowed.

CONCLUSION

Applicant believes Applicant has overcome the Examiner's objections and rejections to Claims 1-30 and 34. Moreover, Applicant believes that pending Claims 1-30, 34, and 76-81 are in a condition for allowance, which Applicant respectfully requests.

Applicant believes this Response should allow the Examiner to allow the above-referenced patent application to issue as a U.S. patent without further amendments to the specification or claims. Thus, Applicant also requests notification to that effect.

If questions should arise, please telephone the undersigned attorney.

EXTENSION OF TERM

The proceedings herein are for a patent application, and the provisions of 37 CFR 1.136 apply. Applicant does not believe this Response requires an extension of time. However, Applicant requests a conditional petition in case Applicant inadvertently overlooked the need to petition for a extension of time, in which case Applicant requests that any and all applicable charges be charged to Applicant's Deposit Account, 232053. Applicant intends this authorization to be carried throughout the pendency of this Application, in full accordance with 37 CFR 1.136.

Respectfully submitted,

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